REAL-TIME VIDEO PROCESSING ON HETEROGENEOUS COMPUTING PLATFORMS - ZYNQ SoC

WHEN
September 11th - 12th, 2019

DURATION
10h - Certificate of Attendance

LECTURER
Tomasz Kryjak, PhD
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WHERE
FCT-UNL - Building X

AUDIENCE
Students and Professors

REGISTRATION
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AGH

Erasmus+

FACULDADE DE CIÊNCIAS E TECNOLOGIA
UNIVERSIDADE NOVA DE LISBOA

PROGRAM

DAY 1
Lecture:

Introduction to FPGA and Zynq SoC.

Overview sample application - Traffic Sign Detection

Laboratory:

FPGA Hello World (Vivado IDE)

Zynq Hello World

Video pass-through (HDMI (Laptop) - Zybo board - HDMI (LCD))

Thresholding

Median filtering

Centroid and bounding box Computation and Visualization

DAY 2
Lecture:

Selected computer vision systems implemented in FPGA and Zynq SoC

Laboratory:

Zynq PS-PL communication via AXI Registers

Zynq PS-PL communication via AXI BRAM Controller

Interrupts - to execute the program on the processor when data is ready

Integrating the whole application (Traffic Sign Detection)